

Solutions - Quiz 3

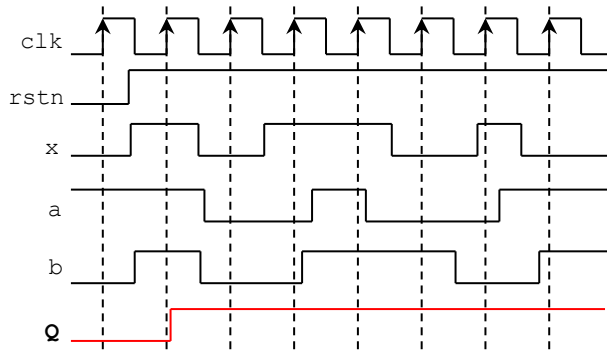
(November 8th @ 5:30 pm)

PROBLEM 1 (30 PTS)

- Complete the timing diagram of the circuit whose VHDL description is shown below:

```
library ieee;
use ieee.std_logic_1164.all;
```

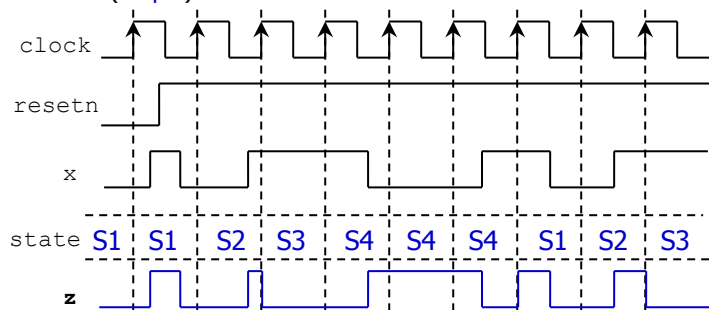
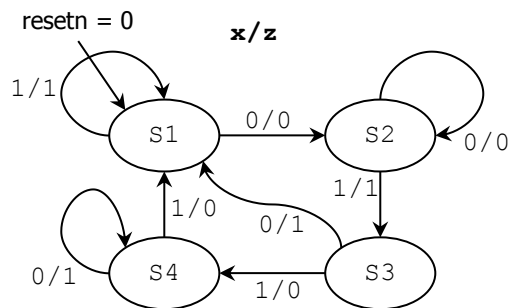
```
entity circ is
  port ( rstn, a,b, x, clk: in std_logic;
        q: out std_logic);
end circ;
```



```
architecture xst of circ is
  signal qt: std_logic;
begin
  process (rstn, clk, a, b, x)
  begin
    if rstn = '0' then
      qt <= '0';
    elsif (clk'event and clk = '1') then
      if x = '1' then
        qt <= a xnor b;
      end if;
    end if;
  end process;
  q <= qt;
end xst;
```

PROBLEM 2 (35 PTS)

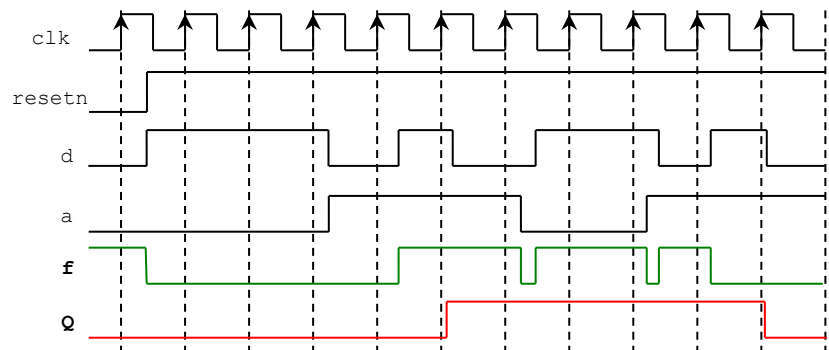
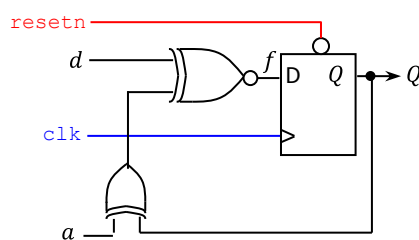
- Complete the timing diagram of the following state machine: (30 pts)



- For the given FSM diagram, circle or mark the correct FSM type: ~~(Mealy)~~ (Moore)

PROBLEM 3 (35 PTS)

- Given the following circuit, complete the timing diagram and get the excitation equation for Q.



$$Q(t+1) \leftarrow \overline{a \oplus Q(t)} \oplus d$$